

<b>Notice of References Cited</b>	Application/Control No. 09/880,699	Applicant(s)/Patent Under Reexamination TAKAHASHI, RICHARD J.	
	Examiner Tracey Akpati	Art Unit 2135	Page 1 of 1

**U.S. PATENT DOCUMENTS**

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
	A	US-			
	B	US-			
	C	US-			
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**FOREIGN PATENT DOCUMENTS**

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**NON-PATENT DOCUMENTS**

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	Sherigar et al. A Pipelined Parallel Processor to Implement MD4 Message Digest Algorithm on Xilinx FPGA. 1/1998. pgs 394-399
	V	
	W	
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\*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)  
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